IN THE CLAIMS

1. (Currently Amended) A semiconductor integrated circuit having nonvolatile memory cells each of which comprises one memory transistor, two switch transistors and two diffusion-layer lines, wherein said memory transistor includes a gate insulating film having discrete traps and a memory gate electrode connected to a word line, said two diffusion-layer lines constitute a source line and a bit line, ~~and~~ the switch gate electrodes of said two switch transistors are extended along said source line and said bit line, said two switch transistors are formed between said two diffusion-layer lines, said memory transistor is formed between said two switch transistors and each channel of said one memory transistor and said two switch transistors is formed continuously at the portion between said two diffusion-layer lines.

2-14. (Canceled)

15. (New) A semiconductor integrated circuit having a memory cell array comprising:

a semiconductor substrate having a main surface;

a plurality of word line formed over said main surface and extending in a first direction;

a plurality of bit line/source line formed in said semiconductor substrate and extending in a second direction, perpendicular said first direction; and

a plurality of nonvolatile memory cell each of which is formed between adjacent two of said bit line/source line and below said word line, and comprises two diffusion layers connected to the corresponding bit line/source line, first and second switch transistors and one memory transistor formed between said first and second switch transistors,

wherein said memory transistor includes a gate insulating film having discrete traps and a memory gate electrode connected to said word line,

wherein said first switch transistor includes first switch gate electrode,

wherein said second switch transistor includes second switch gate electrode,

wherein one nonvolatile memory cell shares said bit line/source line with the other nonvolatile memory cell which is neighboring to one nonvolatile memory cell in said first direction,

wherein said first switch g ate electrode of one nonvolatile memory cell is extended along said bit line/source line and connected to said first switch gate electrode of the

other nonvolatile memory cell which is neighboring tone nonvolatile memory cell which is neighboring to one nonvolatile memory cell in said second direction,

wherein said second switch gate electrode of one nonvolatile memory cell is extended along said bit line/source and connected to said second switch gate electrode of the other nonvolatile memory cell which is neighboring to one nonvolatile memory cell in said second direction, and,

wherein first channel of said first switch transistor, second channel of said memory transistor and third channel of said second switch transistor are formed continuously at the portion of said semiconductor substrate between said two diffusion layers.

16. (New) A semiconductor integrated circuit according to claim 15,

wherein two edges of said gate insulating film having discrete traps memorize one bit information respectively, and

wherein said nonvolatile memory cell memorizes two bit information.

17. (New) A semiconductor integrated circuit according to claim 16, wherein said nonvolatile memory cell has an area of $8F^2$, and an area for one bit information is $4F^2$.

18. (New) A semiconductor integrated circuit according to claim 16,

wherein each of said first and second switch gate electrodes consists of side wall gate electrode, and said nonvolatile memory cell has an area smaller than $8F^2$.

19. (New) A semiconductor integrated circuit according to claim 15,

wherein said gate insulating film having discrete traps includes a silicon nitride film.